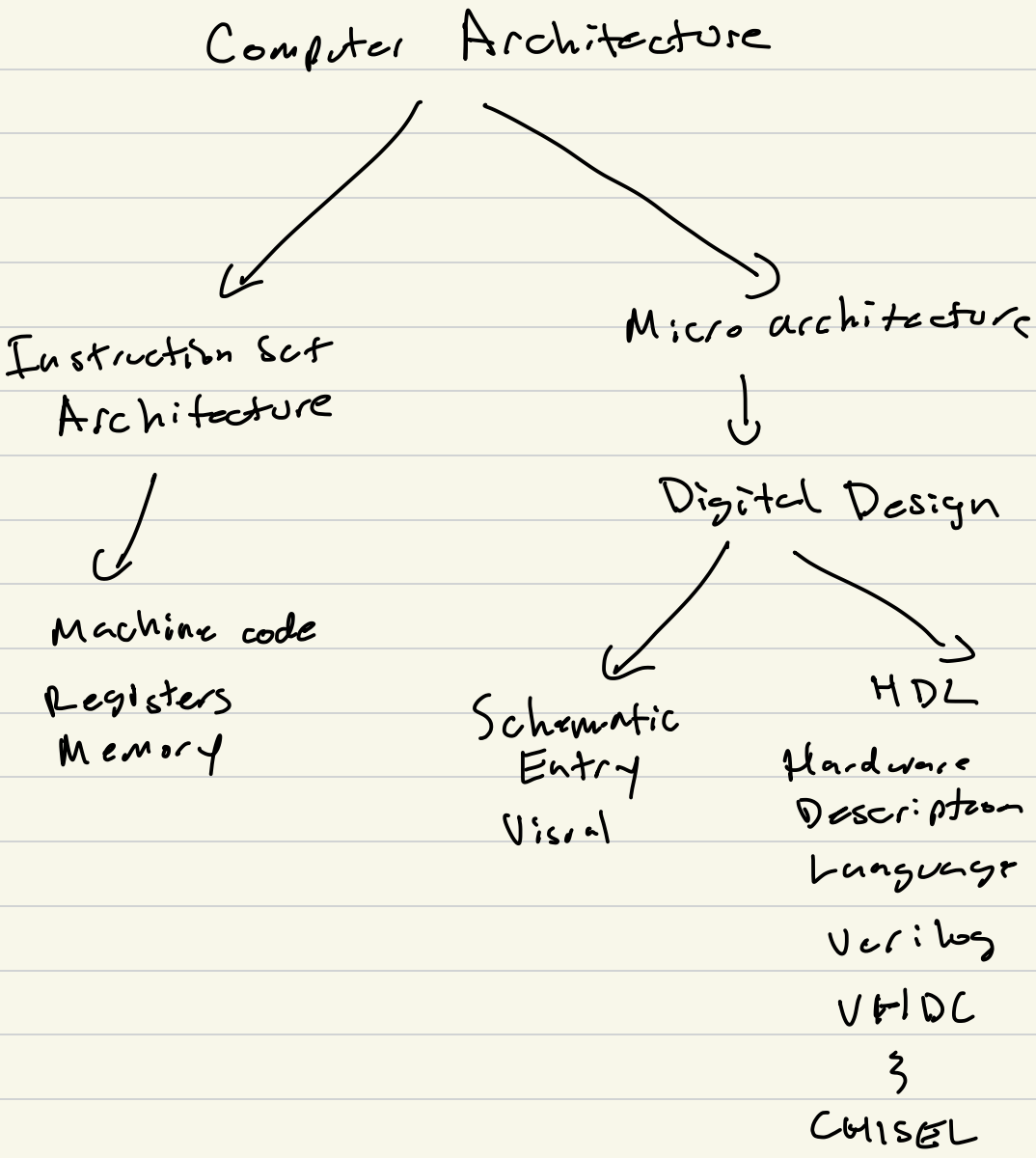
CS 315-01 Processor Design Components

C coding
Data representation
Memory
RISC-V Assembly
RISC-V Machine Code
RISC-V Emulator
Cache Design
Digital Design

Processor Design
- Instruction Set Architecture (ISA)
- Micro architecture


Computer Architecture
Instruction Set Architecture
Machine code
Registers
Memory
Micro architecture
Digital Design
Schematic Entry
Visual
HDL
Hardware Description Language
Verilog
VHDL
&
CHISEL

Processor Design

Moore's Law

The number of transistors doubles every 1.5 years.

↑

increased size

increased density

Two micro architecture

single-cycle processor

→ Pipelined Processor

This class

Super scalar

Out of order execution

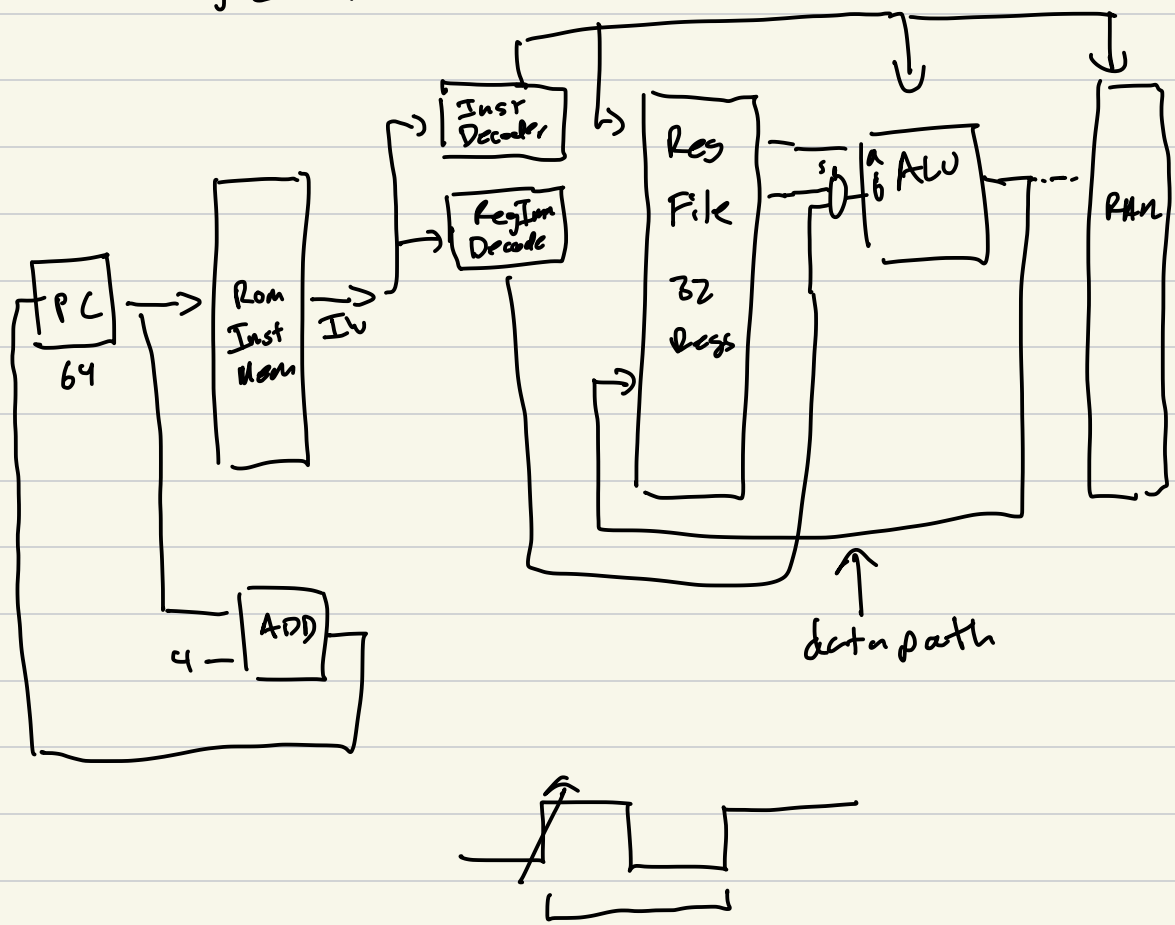
Speculative execution

Lab 05 → Lab 06 → Project 06

↑

single-cycle RISC-V

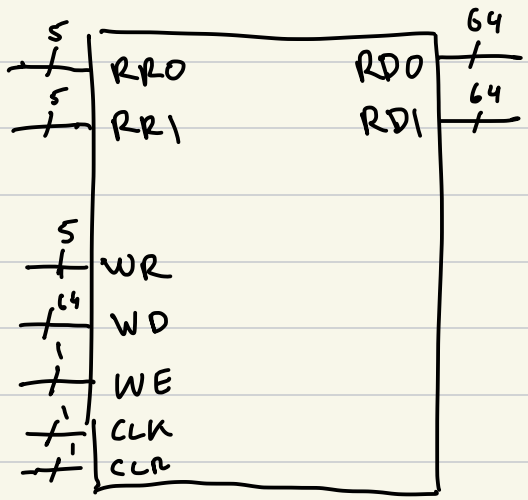
Single Cycle Processor



Register File

32 64-bit Registers $x0, x1, \ldots, x31$

Read up to two register values on a single clock cycle and we write to one register. x0 (zero) will always be 0, cannot update.



RR - read reg #

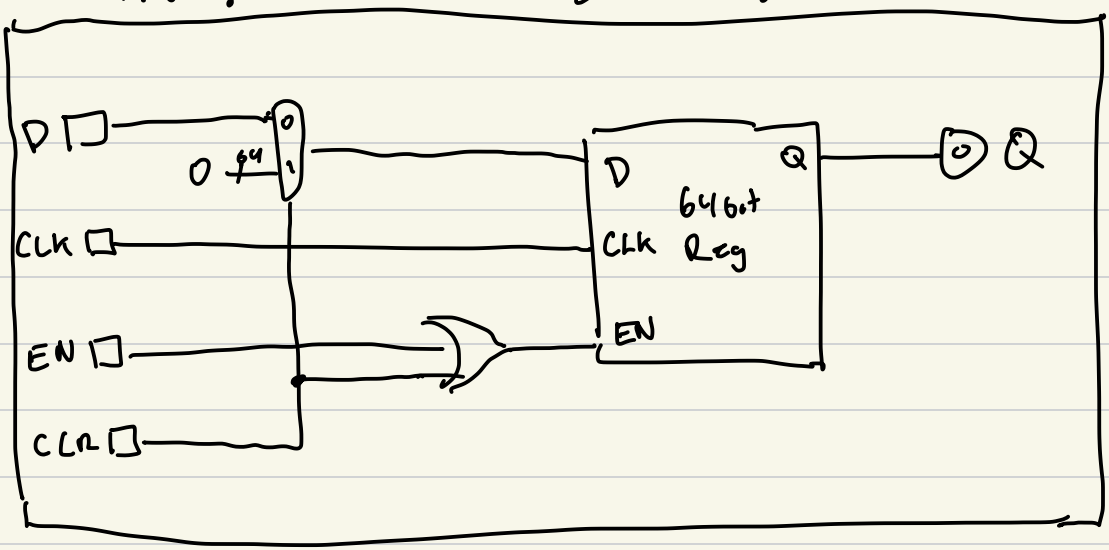
RD - read data

WR - write register

WD - write data

WE - write enable

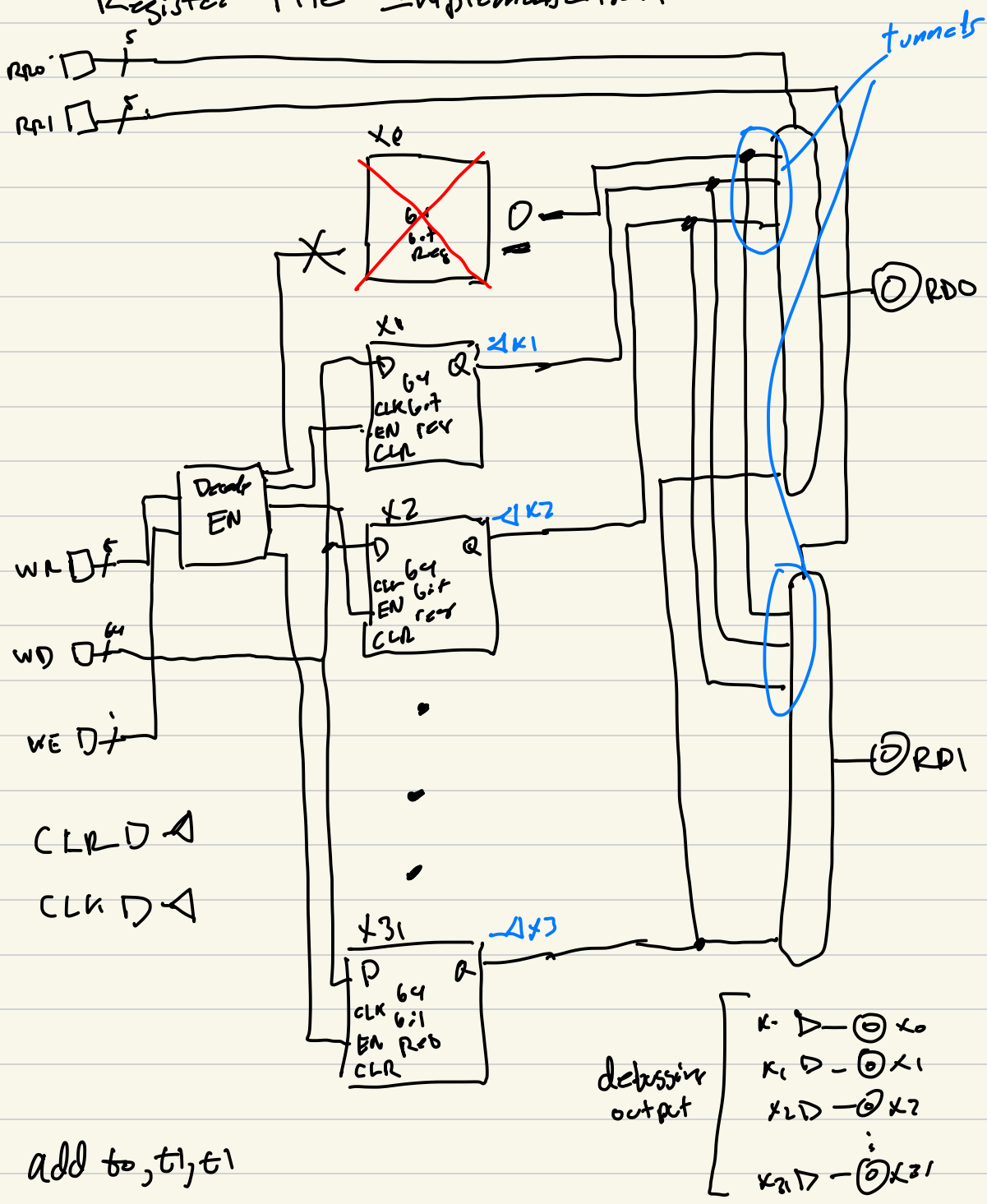
Adding CLR to Digital Register



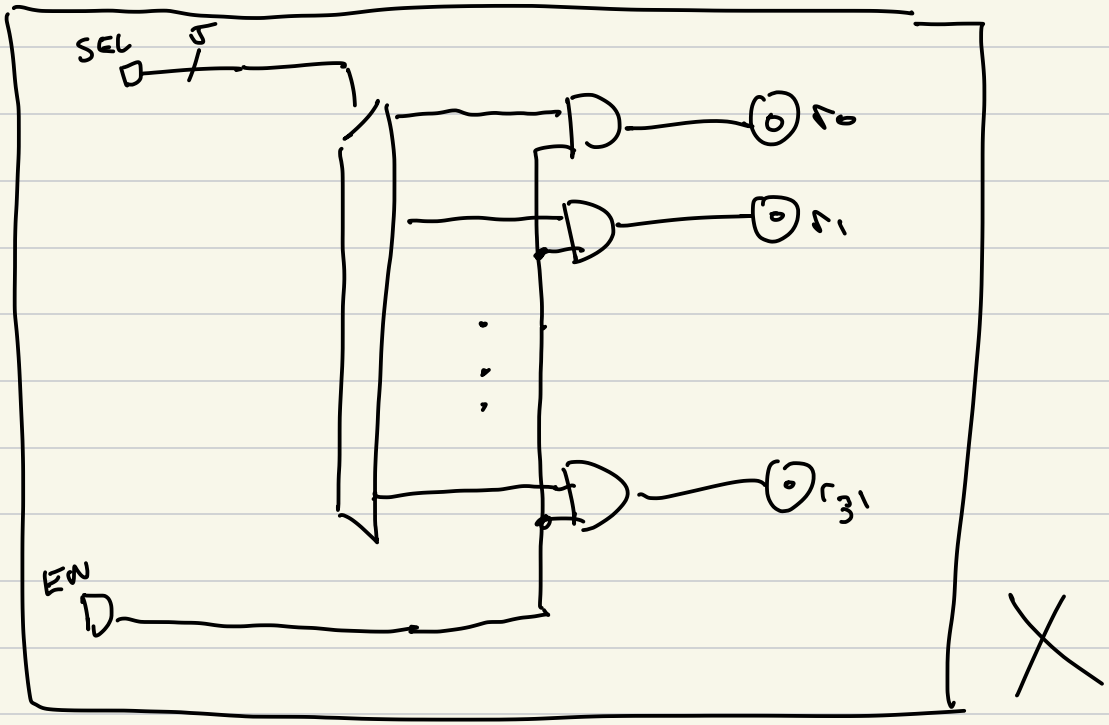
64 b.t Reg with CLR

Synchronous
Clear

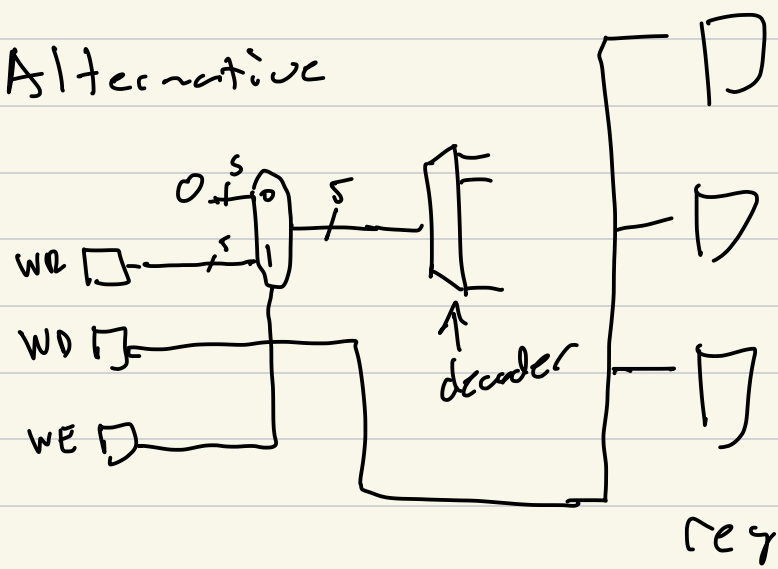
Register File Implementation

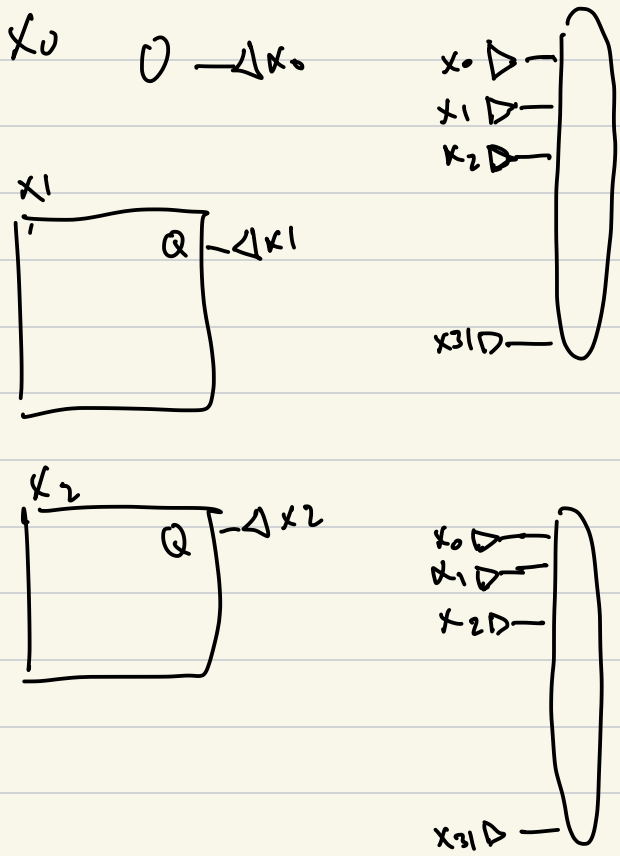


Decoder with EN



Alternative




x0
0
x0
x1
Q
x1
x2
Q
x2
x0
x1
x2
x31
x31